What is claimed is:

1. A nonvolatile semiconductor memory device comprising a memory cell array including a plurality of memory cells disposed in a row direction and a column direction,

wherein each of the memory cells includes a source region, a drain region, a channel region between the source region and the drain region, a word gate, a select gate, and a nonvolatile memory element formed between the word gate and the channel region, the word gate and the select gate being disposed to face the channel region,

wherein the memory cell array includes:

a plurality of word lines each of which is commonly connected with the word gates of the memory cells in each row;

a plurality of bit lines each of which is commonly connected with the drain regions or the source regions of the memory cells in each column;

a word line driver section which drives the word lines; and

a bit line driver section which drives the bit lines,

wherein the word line driver section includes a plurality of unit word line driver sections, and

wherein each of the unit word line driver sections drives two of the word lines connected respectively with two of the word gates adjacent to each other in the column direction.

2. The nonvolatile semiconductor memory device as defined in claim 1,

wherein the two word lines driven by each of the unit word line driver sections are short-circuited.

3. The nonvolatile semiconductor memory device as defined in claim 1,

wherein each of the memory cells includes a first region adjacent to the source region and a second region adjacent to the drain region in the channel region, and

wherein the select gate is disposed over the first region and the word gate is disposed over the second region with the nonvolatile memory element interposed in-between.

4. The nonvolatile semiconductor memory device as defined in claim 1,

wherein each of the memory cells includes a first region adjacent to the source region and a second region adjacent to the drain region in the channel region, and

wherein the word gate is disposed over the first region with the nonvolatile memory element interposed in-between and the select gate is disposed over the second region.

5. The nonvolatile semiconductor memory device as defined in claim 1,

wherein the memory cell array includes:

a plurality of select lines each of which is commonly connected with the select gates of the memory cells in each row; and

a select line driver section which drives the select lines,

wherein the select line driver section includes a plurality of unit select line driver sections, and

wherein at least one of the unit select line driver sections drives two of the select lines connected respectively with two of the select gates adjacent to each other in the column direction.

6. The nonvolatile semiconductor memory device as defined in claim 5,

wherein the two select lines driven by at least one of the unit select line driver sections are short-circuited.

7. The nonvolatile semiconductor memory device as defined in claim 1,

wherein the nonvolatile memory element is formed of an ONO film which includes two oxide films (O) and a nitride film (N) between the two oxide films (O).